12/06/2002 09/992,387

12jun02 12:31:20 User267149 Session D139.1

SYSTEM:OS - DIALOG OneSearch
File 344:CHINESE PATENTS ABS APR 1985-2002/APR
(c) 2002 EUROPEAN PATENT OFFICE
File 347:JAPIO Oct 1976-2002/Feb(Updated 020604)
(c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.
File 351:Derwent WPI 1963-2002/UD,UM &UP=200236
(c) 2002 Thomson Derwent
*File 351: Please see HELP NEWS 351 for details about U.S. provisional
applications.
File 371:French Patents 1961-2002/BOPI 200209
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File 350:Derwent WPIX 1963-2002/UD,UM &UP=200236
(c) 2002 Thomson Derwent
*File 350: Please see HELP NEWS 350 for details about U.S. provisional
applications. Also more updates in 2002.

12/06/2002 09/992,387

Set	Items	Description
S1	9217	(BALL()GRID OR BGA OR LAND()GRID OR PAD()GRID OR PIN()GRID-)(3N)ARRAY? ?
S2	1233	INTERCONNECT??????(3N)DENSIT?????
S3	291265	INTEGRAT??????(2N)(CIRCUIT??? OR IC)
S4	51380	100(W)(MU OR MICRON? ?)
S5	1999	(MU OR MICRON? ?)(3N)(CENTER? ? OR CENTR?????)
S6	2147	PITCH???(3N)(MICRON? ? OR MU)
S7	1205	CENTER? ?(1W)CENTER? ?
S8	391	PITCH???(2N)CENTER? ?
S9	56628	S4:S8
S10	49770	ACTIVE(3N)SURFACE? ?
S11	967	PASSIVE(3N)SURFACE? ?
S12	2571127	ELECTRIC???
S13	891706	(COUPL??? OR CONNECT??? OR LINK??? OR JOIN???)(3N)(MEMBER? ? OR UNIT? ? OR PART? ?)
S14	5123739	FILM??? OR LAYER??? OR COAT??? OR SUBSTRAT?????
S15	1196023	INSULAT????? OR MC=U11-C08A6
S16	1496	INTERPOSER? ?
S17	2385696	POLYIMIDE? ? OR POLYIMIDO OR RESIN OR EPOX??? OR (HEAT??? - OR WEAR OR CORROSION???)(4N)RESIST???????
S18	0	MC=VO4-R07C
S19	19896	IMIDO OR IMIDE???(2N)POLYMER???
S20	45261	WIRE? ?(2N)(BOND??? OR BALL? ?)
S21	45405	(SOLDER??? OR FUSIBLE(2N)ALLOY? ? OR BOND???? OR JOIN?????? OR CEMENT????)(5N)(BALL? ? OR BUMP? ?)
S22	1363	(COPPER OR CU)(5N)(BALL? ? OR BUMP? ?)
S23	584	(NICKEL OR NI)(5N)(BALL? ? OR BUMP? ?)
S24	140	(PALLADIUM OR PD)(5N)(BALL? ? OR BUMP? ?)
S25	68594	TAPE()AUTOMAT???(1N)BOND??? OR TAB
S26	8794	FLIP()CHIP OR FLIP()BOND
S27	117027	THERMOSETTING? ? OR THERMOPLASTIC???(3N)(BLEND??? OR MIX OR MIXTURE OR MIXING)
S28	8246	THERMO()COMPRESSION??? OR THERMOCOMPRESSION??? OR INTERDIF-FUSION??? OR INTER()DIFFUSION???
S29	125008	S27 OR S28
S30	62688	ENCAPSULAT?????? OR CAPSULAT??????
S31	381	S1 AND S30
S32	15	S31 AND S25
S33	0	S32 AND S9
S34	12	S32 AND (S17 OR S19)
S35	0	(S4 OR S5 OR S6 OR S7) AND S16
S36	20084	(S4 OR S5 OR S6 OR S7) AND (S17 OR S19)
S37	1274	MC=V04-R07C
S38	2395822	S17,S19,S37
S39	7018	MC=U11-E01C
S40	12472	S26,S39
S41	7018	S40 AND S39
S42	166	S41 AND S30
S43	20	S42 AND S15
S44	0	S43 AND S16
S45	12	S43 AND S3
S46	12	IDPAT (sorted in duplicate/non-duplicate order)
S47	6	IDPAT (primary/non-duplicate records only)

S48	306	S9 AND (S10 OR S11)
S49	21	S48 AND S15
S50	0	S49 AND S16
S51	2	S49 AND S20
S52	0	S49 AND (S21 OR S22 OR S23 OR S24)
S53	0	S49 AND GOLD(3N)(BUMP??? OR BALL???)
S54	0	S49 AND S29
S55	21	S49 AND S4
S56	0	S55 AND S5
S57	21	IDPAT S55 (sorted in duplicate/non-duplicate order)
S58	14	IDPAT S55 (primary/non-duplicate records only)
S59	130	S1 AND S16
S60	65	S59 AND S21
S61	3	S60 AND S22
S62	1302	S29 AND S30
S63	0	S62 AND (INTERCONNECT??????(3N)DENSIT?????)
S64	10	S62 AND S10
S65	2	S64 AND S40

34/3,AB/1 (Item 1 from file: 351)
DIALOG(R)File 351:Derwent WPI

013192417
WPI Acc No: 2000-364290/200031
XRAM Acc No: C00-109842
XRPX Acc No: N00-272620

Integrated circuit package e.g. **ball grid array** package has flex tape which has conductive metal lead pattern positioned on side of tape facing substrate with apertures, exposes lead pattern for solder ball bonding

Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: ALAGARATNAM M; CHIA C J; LOW Q H

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6057594	A	20000502	US 97842379	A	19970423	200031	B

Priority Applications (No Type Date): US 97842379 A 19970423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6057594	A		5	H01L-023/495	

Abstract (Basic): US 6057594 A
Abstract (Basic):

NOVELTY - IC package has molded plastic base structure sandwiched between heat conductive substrate (4) and flex tape (16). Flex tape has conductive metal lead pattern (18) positioned on tape side facing substrate with apertures (22) that exposes lead pattern for solder ball bonding. Semiconductor IC (12) is mounted on central point of heat spreader (10). Chip and wiring bonding are then **encapsulated** on substrate.

DETAILED DESCRIPTION - A molded plastic base structure includes heat conductive substrate and flex tape extending from corresponding side of substrate. The heat conductive substrate is laminate structure comprising metal and ceramics. The molded plastic material is present between substrate and flex tape which has conductive metal lead pattern on the tape side which faces the substrate. Apertures exposes conductive lead pattern for solder ball bonding. A semiconductor IC chip with active and non-active side is mounted to central portion of heat spreader and active side has bond pads (14) for interconnecting integrated circuit. Wire bonding interconnects bond pads on clip to metal lead pattern chip. The wire bonding are then **encapsulated** on substrate by filling cavity in the substrate partially by a **resin**. The cavity has molded plastic along its side walls. The flex tape also extends along side walls of cavity.

USE - For large scale integrated (LSI) circuits, integrated circuit (IC) packages e.g. **ball grid array** (**BGA**) package, formed by **tape automated bonding** (**TAB**).

ADVANTAGE - As chip is directly fixed to heat spreader heat dissipation is increased. Wire bonding is lower in cost and has flexibility higher then **tape automated bonding** (

TAB) hence resulting package is economical to manufacture, thin and light weight.

DESCRIPTION OF DRAWING(S) - The figure shows perspective view of **ball grid array** package.

Heat conductive substrate (4)
Heat spreader (10)
Semiconductor integrated chip (12)
Bond pads (14)
Flex tape (16)

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34/3,AB/2 (Item 2 from file: 351)
DIALOG(R)File 351:Derwent WPI

012180204
WPI Acc No: 1998-597117/199851
XRAM Acc No: C98-179352
XRPX Acc No: N98-464724
Thin power tape **ball grid array** package - has semiconductor chip mounted in heat spreader recess and its bonding pads connected to metal interconnect patterns on flex tape
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: ALAGARATNAM M; CHIA C J; VARIOT P
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 880175	A2	19981125	EP 98303039	A	19980421	199851	B
JP 11003957	A	19990106	JP 98109632	A	19980420	199911	
US 5869889	A	19990209	US 97840614	A	19970421	199913	

Priority Applications (No Type Date): US 97840614 A 19970421
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 880175	A2	E	5	H01L-023/13	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 11003957	A		4	H01L-023/12	
US 5869889	A			H01L-023/34	

Abstract (Basic): EP 880175 A

Package comprises a heat conductive support (10) formed to have a recessed portion with opposing planar surfaces (12,14) and a centrally disposed surface (16). Flex tape is attached to the planar surfaces (12,14) and extends to the centrally disposed surface (16). The flex tape includes one or more metal interconnect patterns (22) on an exposed surface. Semiconductor integrated circuit chip (24) is mounted on centrally disposed surface (16) spaced from the flex tape (18,20). Chip (24) has bonding pads (26). Wire bonds interconnect pads (26) to the interconnect pattern (22). Preferably chip (24) and the wire bonds are **encapsulated** by plastic molding or **epoxy** on the heat conductive support (10). Preferably the metal interconnect pattern (22) is connected by solder balls to a mother board.

USE - Flex tape **ball grid array** package where the flex tape and a formed heat spreader provide the package substrate.

ADVANTAGE - The use of flex tape for the substrate is cheaper to manufacture than laminates and ceramics and the wire bonding for the interconnect of the chip and the substrate is lower in cost has higher flexibility than other interconnects such as **TAB** bonding. The recess or cavity for attachment of the chip to the heat spreader allows for greater protection of the chip and easier assembly of a thin and light package.

34/3,AB/3 (Item 3 from file: 351)
DIALOG(R)File 351:Derwent WPI

011556346
WPI Acc No: 1997-532827/199749
XRAM Acc No: C97-170101
XRPX Acc No: N97-443738
Liquid **resin** encapsulant for **encapsulating** semiconductor devices - based on naphthalene **polyepoxy resin**, hardener and silica powder
Patent Assignee: TOSHIBA CHEM CORP (TOSM)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9255763	A	19970930	JP 9693600	A	19960322	199749	B

Priority Applications (No Type Date): JP 9693600 A 19960322
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9255763	A		4	C08G-059/24	

Abstract (Basic): JP 9255763 A

An **encapsulated** semiconductor device comprises a device which is **encapsulated** with a cured substance of a liquid **resin** encapsulant consisting of (A) an **epoxy resin** containing a naphthalene skeleton, (B) a hardener, and (C) a silica powder.

Also claimed is a liquid **resin** encapsulant which comprises essential components of (A) an **epoxy resin** containing naphthalene skeleton, (B) a hardener, and (C) a silica powder.

USE - This is used in PPGA (plastic **pin grid array**) and **TAB** (**tape automated bonding**).

ADVANTAGE - This encapsulant has good adhesion, moisture **resistance**, **heat resistance**, electric properties, and workability such as flowability, and no occurrence of voids and cracks, giving a device having little warp and high reliability.

34/3,AB/4 (Item 4 from file: 351)
DIALOG(R)File 351:Derwent WPI

010581359
WPI Acc No: 1996-078312/199609
XRAM Acc No: C96-025943
XRPX Acc No: N96-065175

PCB mounting applications of an **encapsulated** semiconductor package - comprises IC, connection leads and conducting layer sealed in thin layer of waterproof, moulded **resin** that has only solder bumps or other types of appropriate connectors for device mounting showing.

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: UEDA T

Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19526511	A1	19960125	DE 1026511	A	19950720	199609	B
JP 8037253	A	19960206	JP 94171020	A	19940722	199615	
KR 201168	B1	19990615	KR 9522303	A	19950722	200060	

Priority Applications (No Type Date): JP 94171020 A 19940722
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19526511	A1		32	H01L-023/50	
JP 8037253	A		22	H01L-023/12	
KR 201168	B1			H01L-023/04	

Abstract (Basic): DE 19526511 A

For a device (1) configured for surface mounting the IC (2), connecting pads (3), and the interconnecting leads (4) joined to the pads are all within the surface of the **resin** (6) with only the solder bumps (5) that are connected to the leads (4) showing through the surface of the mould. The **resin encapsulation** may also be used for devices configured for bump-grid **array** (**BGA**), zig=zag or ZIP, SVP or other PCB mounting methods, in each case only the appropriate device supports and connectors being accessible outside the **resin** mould for reflow soldering to the PCB surface. The method may also be used with **TAB** IC's.

USE - The device may be used in a wide range of manufacturing and PCB mounting applications.

ADVANTAGE - Gives high packing density, reliability and excellent damp resistance and protection from external effects.

34/3,AB/5 (Item 5 from file: 351)
DIALOG(R)File 351:Derwent WPI

008100608
WPI Acc No: 1989-365720/198950
XRAM Acc No: C89-162127
XRPX Acc No: N89-278201
Controlling distribution of curable **resin** on substrate - by forming dam of cured **resin** using predetermined radiation pattern
Patent Assignee: DOW CORNING CORP (DOWO)
Inventor: ECKSTEIN M H; LUTZ M A
Number of Countries: 011 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 345979	A	19891213	EP 89305369	A	19890526	198950	B
AU 8936144	A	19891214				199005	
BR 8902723	A	19900123				199009	
JP 2017975	A	19900122	JP 89131724	A	19890526	199009	
ES 2014652	A	19900716	ES 89890201	A	19890608	199033	
US 4961886	A	19901009	US 88204436	A	19880609	199043	
EP 345979	B1	19940608	EP 89305369	A	19890526	199422	
DE 68915860	E	19940714	DE 615860	A	19890526	199428	
			EP 89305369	A	19890526		
CA 1336702	C	19950815	CA 599781	A	19890516	199542	

Priority Applications (No Type Date): US 88204436 A 19880609
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 345979	A	E	11		
Designated States (Regional): DE FR GB IT NL					
EP 345979	B1	E	11	B29C-041/36	
Designated States (Regional): DE FR GB IT NL					
DE 68915860	E			B29C-041/36	Based on patent EP 345979
CA 1336702	C			B29C-041/36	

Abstract (Basic): EP 345979 A

Flow of a flowable radiation curable material (26) is restricted by forming a dam (40) of the material by exposing a portion of it to radiation of sufficient intensity to cause it to cure.

The flowable material is dispensed onto a substrate and a predetermined area of the substrate is exposed to radiation to form a dam of cured material before the remainder of the material is exposed to the same radiation to cure it.

USE/ADVANTAGE - Process is used to make plastic bosses on substrates and can be used to coat and/or **encapsulate** printed circuit boards, plastic **pin grid arrays, tape automated bonding** devices, hybrid circuit substrates, chip on board **encapsulation**, and **encapsulation** of devices contg. holes which are to remain free of material.

34/3,AB/6 (Item 6 from file: 351)
DIALOG(R)File 351:Derwent WPI

007615995
WPI Acc No: 1988-249927/198835
XRPX Acc No: N88-190365
Integrated circuit plastic **pin grid array** mfg. process - inserting terminal pins into holes in interconnect tape, and moulding in encapsulant **resin**
Patent Assignee: OLIN CORP (OLIN)
Inventor: ARMER T A; BRIDGES W G; CHANG K; CHANG K S
Number of Countries: 032 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8806395	A	19880825	WO 88US384	A	19880210	198835	B
AU 8812989	A	19880914				198849	
US 4816426	A	19890328	US 8752327	A	19870521	198915	
EP 382714	A	19900822	EP 88902047	A	19880210	199034	
JP 2502322	W	19900726	JP 88501929	A	19880210	199036	
US 4965227	A	19901023	US 88145977	A	19880202	199045	
US 5144412	A	19920901	US 8716614	A	19870219	199238	
			US 8752327	A	19870521		
			US 88145977	A	19880202		
			US 90562281	A	19900802		
PH 28943	A	19950613	PH 36494	A	19880212	199902	
KR 9610011	B1	19960725	WO 88US384	A	19880210	199922	
			KR 88701166	A	19880924		

Priority Applications (No Type Date): US 88145977 A 19880202; US 8716614 A 19870219; US 8752327 A 19870521; US 90562281 A 19900802
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4816426	A		21		
US 4965227	A		25		
US 5144412	A		37	H01L-023/02	CIP of application US 8716614
					CIP of application US 8752327
					Div ex application US 88145977
					CIP of patent US 4816426
					Div ex patent US 4965227

Abstract (Basic): WO 8806395 A

The interconnect tape (18') with pins (26a) inserted is **encapsulated** in a body (270) of polymeric **resin**. Pref. of the outer surface (272) is occupied by the heat sink (106) with a base (247) exposed flush with the surface or raised or recessed. After removal from the mould, the package receives a semiconductor chip)82) attached (273) to the interior base (245) of the heat sink (106) and wire-bonded or connected by **tape automated bonding** to leads (21).

The enclosure (278) is sealed by a lid (276) with an adhesive or solder ring (280). The tape (18') is supported on shoulders (39') and the collar (108) of the heat sink.

ADVANTAGE - Package can be mfd. with efficiently operated

automated assembly, and single moulding step, prior to which **TAB** tape with chip attached can be tested.

Abstract (Equivalent): US 5144412 A

Pin grid array package for housing an integrated circuit comprises an interconnect tape defining a metal interconnect circuit pattern, and holes in the pattern into each of which a terminal pin is inserted. The pin heads are slightly larger than the holes to mechanically lock the tape. A polymer **resin**, e.g. polyphenylsulphide, polysulphone, polyethersulphone, polyarylether, polyamide, polyether ketone or polyetherimide, **encapsulates** each head.

ADVANTAGE - Low cost automatic assembly.

US 4965227 A

The process for forming an integrated circuit **pin grid array** package, comprises the steps of providing an interconnect tape having first and second opposing surfaces, the first surface having a metal circuit pattern defining a number of leads forming a set of holes of a first diameter in the metal circuit pattern. The insertion end of a pin is inserted into a first fixture. Interconnect tape is placed over the pin head end such that the holes in the circuit pattern encircle the pin heads and be the interconnect tape rests on the first shoulder of the pins. Pins are soldered to the interconnect tape using a mask to control the solder.

The cavity is filled with a polymer **resin** so as to at least partially surround and support the pins and tape and thereby form the plastic **encapsulated pin grid**

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014416194
WPI Acc No: 2002-236897/200229
Related WPI Acc No: 2002-224860
XRAM Acc No: C02-071629
XRPX Acc No: N02-182211
Method of making **integrated circuit** package comprises forming die pad and leads on substrate having apertures, mounting **integrated circuit** device on die pad, connecting device to leads with bond wires and **encapsulating** bond wires and device
Patent Assignee: AMKOR TECHNOLOGY INC (AMKO-N)
Inventor: DARVEAUX R F; FUSARO J M; RODRIGUEZ P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6331451	B1	20011218	US 99434546	A	19991105	200229	B

Priority Applications (No Type Date): US 99434546 A 19991105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6331451	B1		21	H01L-021/58	

Abstract (Basic): US 6331451 B1
Abstract (Basic):

NOVELTY - Method of making **integrated circuit** package comprises: forming planar metal die pad and metal leads on **insulating** substrate having apertures; mounting an **integrated circuit** device on the die pad; connecting the **integrated circuit** device to the leads with bond wires; and applying an encapsulant to cover the bond wires and **integrated circuit** device and fill the apertures.

DETAILED DESCRIPTION - Method of making **integrated circuit** package involves providing a planar **insulative** substrate having first apertures (32) between its first and second surfaces. A planar metal die pad (11) and planar metal leads (14, 14A) are arranged on the second surface of the substrate. The first surfaces of the die pads and leads are on the second surface of the substrate and the first apertures are juxtaposed with the first surface of a lead. An **integrated circuit** device (22) is mounted adjacent the first surface of the die pad. Bond wires (24) are conductively connected between the **integrated circuit** device and the first surface of a lead through the first aperture juxtaposed with that respective lead. An encapsulant material is applied onto the first surface of the substrate so as to cover the bond wires and the **integrated circuit** device and fill the first apertures so that the second surfaces of the die pad, leads, and substrate are exposed at a first surface of the package.

INDEPENDENT CLAIMS are also included for the following:

(i) a method of making a number of **integrated circuit** packages;

(ii) a method of making a **flip chip integrated circuit** package;

(iii) a method of making a substrate for making an **integrated circuit** package; and

(iv) a method of making a substrate for making a **flip chip integrated circuit** package.

USE - None given.

ADVANTAGE - The **integrated circuit** packages are thinner than conventional packages and have improved thermal performance. The packages and the substrates and the methods of making them are reliable and cost effective because the substrate and packages can be assembled using conventional materials and equipment.

DESCRIPTION OF DRAWING(S) - The drawings illustrate cross-sectional side views of stages of making the package.

Die pad (11)

Lead (14, 14A)

Integrated circuit device (22)

Bond pad (23)

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47/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796913
WPI Acc No: 2001-281125/200129
Related WPI Acc No: 2001-272598
XRAM Acc No: C01-085410
XRPX Acc No: N01-200441
Semiconductor and **flip chip** packages, uses thermo-electrically conductive epoxy resin to connect bond pad to backside of die
Patent Assignee: MINCO TECHNOLOGIES LABS INC (MINC-N)
Inventor: POTTER D R; RODENBECK L R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010000927	A1	20010510	US 9865677	A	19980423	200129 B
			US 2000739071	A	20001218	

Priority Applications (No Type Date): US 9865677 A 19980423; US 2000739071 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010000927	A1		9	H01L-023/48	Div ex application US 9865677 Div ex patent US 6191487

Abstract (Basic): US 20010000927 A1
Abstract (Basic):
NOVELTY - A via (22) electrically connects the terminal and the contact pad (21) on the external (19) and internal (17) sides of the substrate (18) respectively. A die (12) is positioned so that its front side faces the substrate external side. A metallisation layer (26) is formed on the back side (28) of the die. A bond pad (16) between the die and substrate mates with the contact pad. A conductive substance (20) connects the die back side to the bond pad to form an electrical connection from the die back side to the substrate terminal.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the manufacture of a **flip chip** package, a semiconductor chip package, and the manufacture of a semiconductor package.
USE - Manufacturing and connecting semiconductor and **flip chip** packages to printed circuit boards using a back side connection.
ADVANTAGE - The area required for both discrete devices and **integrated circuits** formed from a standard die having back side connections is reduced. There is no need for lead wires extending from the die in a **flip chip** package to the printed circuit board so reducing the space require to connect the device to the remainder of the circuit.
DESCRIPTION OF DRAWING(S) - The drawing shows a side cross-section of the **flip chip** package.
Die (12)
Potting material (14)
Bond pad (16)

Internal sides of the substrate (17)
Substrate (18)
External side of the substrate (19)
Conductive substance (20)
Contact pad (21)
Via (22)
Solder balls (24)
Metallisation (26)
Back side of the die (28)

47/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012890963
WPI Acc No: 2000-062797/200005
Related WPI Acc No: 1999-633333
XRPX Acc No: N00-049142
Radio frequency (RF) shield structure of **integrated circuit** chip package
Patent Assignee: AMKOR TECHNOLOGY INC (AMKO-N)
Inventor: GLENN T P
Number of Countries: 023 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9962119	A1	19991202	WO 99US10852	A	19990517	200005	B
US 6150193	A	20001121	US 96741797	A	19961031	200101	
			US 9883524	A	19980522		

Priority Applications (No Type Date): US 9883524 A 19980522; US 96741797 A 19961031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9962119	A1	E	48	H01L-023/552	
Designated States (National): CA JP KR SG					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6150193	A			H01L-021/44	CIP of application US 96741797 CIP of patent US 5981314

Abstract (Basic): WO 9962119 A1
Abstract (Basic):
NOVELTY - The package (10B) has a polymer based **insulating** encapsulant layer (42) to enclose an IC chip (30) and the upper surface (18) of an **insulating** substrate (12) in which the IC chip is mounted. An electrically conductive shield layer (150) is formed above the encapsulant layer so that the edges (152,43) of the shield layer and the encapsulant layer are coincident with the edges (46) of **insulated** substrate.
DETAILED DESCRIPTION - The shield layer comprises polymer containing electrically conductive filler. The bonding pads (38) of the IC chip are connected with the respective metallic traces (22) on the upper surface of the **insulated** substrate through the bonding wires (40). The IC chip is attached to the **insulating** substrate through a **flip chip** interconnection. The metallic layer on the **insulated** substrate is connected to an external reference voltage. An INDEPENDENT CLAIM is also included for shield structure manufacturing method.
USE - In **integrated circuit** chip package used in electronic devices.
ADVANTAGE - Prevents external radiation from interacting with chip operation. Prevents radiation emission from package that could interfere with other circuit components.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view

of package.
Package (10B)
Insulating substrate (12)
Upper surface (18)
Metallic traces (22)
IC chip (30)
Bonding pads (38)
Bonding wires (40)
Encapsulated layer (42)
Edges of **encapsulated** layer (43)
Edges of **insulated** substrate (46)
Shield layer (150)

47/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012228724
WPI Acc No: 1999-034831/199903
XRAM Acc No: C99-010586
XRPX Acc No: N99-026009
Method of electrical component packaging used at wafer level - by forming a plurality of posts on a substrate active side and depositing a conductive layer to connect each post to a component contact
Patent Assignee: CHIPSCALE INC (CHIP-N)
Inventor: CHEN C; YOUNG J L
Number of Countries: 082 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9852225	A1	19981119	WO 98US9793	A	19980513	199903	B
AU 9873856	A	19981208	AU 9873856	A	19980513	199916	
GB 2341277	A	20000308	WO 98US9793	A	19980513	200015	
			GB 9926807	A	19991115		
US 6051489	A	20000418	US 97855106	A	19970513	200026	
KR 2001012499	A	20010215	KR 99710454	A	19991112	200154	

Priority Applications (No Type Date): US 97855106 A 19970513
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6051489	A			H01L-021/44	

Abstract (Basic): WO 9852225 A

A method (I) for making an electronic component package from a component with a number of contact areas on an active side of a substrate comprises: (a) forming a plurality of posts on the active side; (b) depositing a conductive layer for electrically coupling each contact area to its respective post and for contracting traces on a printed circuit board.

Also claimed is an alternative method to (I) comprising: (a) depositing gold beams over the contacts; (b) depositing a first **insulating** layer over the component covering the beams; (c) coupling a cap to the component covering the **insulating** layer; (d) patterning the cap to form a number of trenches thus defining a number of posts and a centre area and exposing the **insulating** layer over the metal beams; (e) depositing a second **insulating** layer over the component covering the posts and centre area; (f) etching all layers above the beams to at least partially expose them; and (g) depositing a conductive layer over the posts to electrically connect the beams and posts.

Also claimed is a package made according to (I).

USE - Used for electronic component packaging, particularly wafer level processing.

ADVANTAGE - The invention provides a circuit package manufacturable at wafer level which provides flexibility and compliancy. Lead connection size can be tailored to the required purpose and lead connections are not on the die surface thus allowing smaller bond pads/junction areas and minimising stress at the surface. The package

may be **encapsulated** to protect the **circuit** and an **integrated** heat sink may be provide

47/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012191657
WPI Acc No: 1998-608570/199851
Related WPI Acc No: 1997-098910
XRPX Acc No: N98-473305

Integrated circuit packaging method - uses **flip-chip** bonding to attach first wafer having tin solder bumps to second wafer having gold ball bumps followed by resin **encapsulation** and subjects portions of lead fingers exposed from package to final processing step

Patent Assignee: LEI W (LEIW-I)
Inventor: LEI W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 338838	A	19980821	TW 95107022	A	19970704	199851	B

Priority Applications (No Type Date): TW 95107022 A 19970704
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 338838	A		18	H01L-021/60	

Abstract (Basic): TW 338838 A

The method involves forming a lead frame having inner and outer layers by using a through punching technique with the outer layer having several conductive lead fingers and inner layer being used for putting a first wafer on a substrate. The first end edge of the lead finger is extended directionally to the substrate, and the second end edge is located along an opposing direction of the first end edge and all extended outwardly.

The surface of the first wafer has several conductive sheets and tin soldering bumps, covered by an **insulating** layer with **flip chip** bonding used to place a second wafer having several gold ball bumps such that it faces the tin soldering bumps of the first wafer. The gold ball bumps of the second wafer are secured to corresponding tin soldering bumps on the first wafer. Metal leads are bonded to connect the conductive sheet and the lead finger, for providing a conductive path from the first wafer and an outer circuit followed by resin **encapsulation**. Outer portions of the lead fingers are exposed from the package and are subjected to a final processing step to finish the packing procedure.

Dwg.0/3

47/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011668768
WPI Acc No: 1998-085677/199808
XRAM Acc No: C98-028921
XRPX Acc No: N98-068060
Attaching **integrated circuit** component with solder bumps to substrate with bond pads - using anhydride containing flux such as methyl- hexahydro-phthalic anhydride
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: GAMOTA D R; HERTSBERG M; SCHEIFERS S M; WILLE S L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5704116	A	19980106	US 96642708	A	19960503	199808	B

Priority Applications (No Type Date): US 96642708 A 19960503
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5704116	A		5	H05K-003/34	

Abstract (Basic): US 5704116 A

A method for attaching an **integrated circuit** component having solder bumps to a substrate having bond pads comprises: (a) dispensing onto the bond pads a solution containing an anhydride fluxing agent; (b) superposing the **integrated circuit** component onto the substrate so that each of the solder bump rests against one of the bond pads and is held by the fluxing agent; and (c) heating to bond the solder bumps to the bond pads and to vaporise the anhydride compound.

Also claimed is an encapsulant method for attaching an **integrated circuit** component to a substrate.

USE - The process is useful for mounting **integrated circuits**, e.g. on printed circuit boards (especially FR4 board which is formed of a polymer layer laminated onto a ceramic or polymer/glass mesh core) using the **flip-chip** process or a ball grid array package onto bond pads, e.g. made of aluminium coated with a layer of chromium covered with copper.

ADVANTAGE - The anhydride can be vaporised during reflow of the solder bump interconnections, leaving no residue on the board which may interfere with under-filling of the component with a polymeric encapsulant. However, if any anhydride residue remains on the surface of the substrate, it can be readily solubilised into the encapsulant which includes an anhydride hardener similar to the anhydride in the fluxing agent. The substrate surface does not need to be cleaned prior to **encapsulation** and good **encapsulation** adhesion is achieved by incorporating any anhydride residue into the encapsulant. Anhydride fluxing agents provide more reliable connection than those containing acids, since anhydrides are more dielectric than acids and lead to better **insulation** and a lower chance of shorts between leads on the substrate.

51/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

01836249

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 61-050349 [JP 61050349 A]
PUBLISHED: March 12, 1986 (19860312)
INVENTOR(s): NITTA TAKEHISA
OGIUE KATSUMI
OTSUKA KANJI
ONISHI SHINJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-161860 [JP 85161860]
FILED: July 24, 1985 (19850724)
JOURNAL: Section: E, Section No. 421, Vol. 10, No. 209, Pg. 129, July 22, 1986 (19860722)

ABSTRACT

PURPOSE: To prevent any erroneous operation due to .alpha. ray irradiation from happening by a method wherein a semiconductor chip is bonded on a substrate and then multiple electrodes on the chip are connected to corresponding external conductive means simultaneously bonding .alpha. ray shielding sheet on the **surface** of **active** region of semiconductor chip.

CONSTITUTION: A semiconductor chip 14 is bonded on the surface of ceramics-made **insulating** base 10 through the intermediary of an adhesive layer 13 made of Au foil or Au metallized layer while multiple electrodes are electrically connected to corresponding leads 12 by **bonding wires** . An .alpha. ray shielding sheet 17 made of high purity (preferably exceeding 5-9) silicon several **100.mu** .m thick including the thickness of another adhesive layer 16 made of phosphorus silicide glass or lead glass etc. is bonded on the **surface** of **active** region of semiconductor chip 14 before or after **wire bonding** process while a ceramics-made **insulating** cap 18 is bonded on the base 10 through the intermediary of a low melting point glass layer 19.

12/06/2002 09/992,387

58/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013430047
WPI Acc No: 2000-601990/200057
XRAM Acc No: C00-180156
Production of additive-loaded fibers or film, e.g. for making sintered, hollow inorganic membranes, involves co-extruding additive-containing cellulose solutions in amine N-oxide and coagulating combined extrudate
Patent Assignee: OSTTHUERINGISCHE MATERIALPRUEFGESELLSCHA (OSTT-N)
Inventor: SCHULZE T; TAEGER E; VORBACH D
Number of Countries: 023 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200053833	A1	20000914	WO 2000DE552	A	20000224	200057	B
DE 19910012	C1	20010118	DE 1010012	A	19990308	200104	

Priority Applications (No Type Date): DE 1010012 A 19990308
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200053833	A1	G	26	D01F-008/02	
DE 19910012	C1			D01F-002/02	

Designated States (National): CA CN JP KR US
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Abstract (Basic): WO 200053833 A1
Abstract (Basic):
NOVELTY - The production of shaped products, especially filaments or film, from polysaccharides or their derivatives or polyvinyl alcohol involves making at least two solutions of the polymer in amine N-oxide-containing solvent, at least one of which also contains finely-dispersed additive(s), co-extruding the solutions and then coagulating the combined extrudate as usual.
USE - For the production of shaped products, especially fibers or film, useful as special materials based on selected additives, e.g. porous, multilayer, inorganic hollow membranes, multilayer membrane reactors, ceramic matrix composites, conductive multi-component fibers, catalyst supports, ionic conductors etc.
ADVANTAGE - Enables the production of solid or hollow multi-component fibers or film etc. with very different contents of additives selected to give a wide range of special properties in the final sintered product.
DESCRIPTION OF DRAWING(S) - Axial section of a 3-component round die for co-extrusion of additive-containing polymer solutions.
central cylindrical channel (1)
annular channels (2, 3)
pp; 26 DwgNo 1/2

58/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012990101
WPI Acc No: 2000-161953/200015
XRAM Acc No: C00-050822
Fast-curing, condensation-crosslinked silicone material for adhesive or sealant applications contains polysiloxane and amino-, oxime- or alkoxysilane crosslinker
Patent Assignee: HEIDELBERGER BAUCHEMIE GMBH (HEID-N)
Inventor: FUTSCHER M; LUFT W; PAHL H; WERNER L
Number of Countries: 029 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19832688	A1	20000203	DE 1032688	A	19980721	200015	B
WO 200005309	A1	20000203	WO 99EP4801	A	19990708	200015	
EP 1102815	A1	20010530	EP 99934630	A	19990708	200131	

Priority Applications (No Type Date): DE 1032688 A 19980721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19832688	A1		6	C08L-083/04	
EP 1102815	A1	G		C08L-083/04	Based on patent WO 200005309

Abstract (Basic): DE 19832688 A1
Abstract (Basic):
NOVELTY - An acid or basic neutral salt is used as the accelerator in a kit for the production of fast-curing, condensation-crosslinked silicone materials containing a diorganopolysiloxane with functional end groups, an amino-, oxime- or alkoxysilane crosslinker, an accelerator and optionally water, fillers, additives and pigments.
DETAILED DESCRIPTION - A kit for the production of fast-curing, aminosilane-crosslinked silicone materials (optionally with fillers, suitable additives and pigments), containing (A) 100 parts by weight (pts. wt.) at least bifunctionally-terminated diorganopolysiloxane with a linear or branched chain comprising repeat units of formula -SiR1R2O- and at least two end groups Z;
Z=H, OH, OR1, -OSiR3(NR4R5)2, -OSi(ON=CR4R5)3 or -OSi(OR3)3;
R1, R2=optionally unsaturated 1-15C hydrocarbyl, possibly substituted with halogen or cyano groups;
(B) 0.1-20 pts. wt. aminosilane crosslinker of formula R3y-Si(NR4R5)4-y or an oxime or alkoxy crosslinker of formula R3-Si(ONCR4R5)4-y or R3-Si(OR3)4-y, in which
R3=H or optionally unsaturated hydrocarbyl or hydrocarbyloxy;
R4, R5=H and/or optionally unsaturated 1-15C aliphatic, cycloaliphatic or aromatic hydrocarbyl, optionally substituted with halogen or CN;
y=0 or 1;
(C) 0.1-20 pts. wt. of an acid or basic neutral salt as accelerator; and
(D) 0-20 pts. wt. water. An INDEPENDENT CLAIM is also included for a process for the production of a sealant or adhesive composition by

mixing (A) with (B) and (C) with (D) and combining the two mixtures just before use.

USE - As a sealant or adhesive or as a molding material (claimed). Applications include bonding metals, glass and plastics, protective coatings for electrical **insulation**, encapsulating materials for electrical and electronic components, impression materials and elastomer moldings.

12/06/2002 09/992,387

58/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008491255
WPI Acc No: 1990-378255/199051
XRAM Acc No: C90-164750
XRPX Acc No: N90-288245
Anhydrite binder for mineral fibres etc. - used in forming heat- or sound-**insulating** coating by spraying
Patent Assignee: SAID H (SAID-I)
Inventor: SAID H; SAID P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2646416	A	19901102	FR 895727	A	19890428	199051	B

Priority Applications (No Type Date): FR 895727 A 19890428

Abstract (Basic): FR 2646416 A
Binder (I) for mineral fibres or other **insulating** prods. for forming **insulating** coating by spraying comprises anhydrite (II).
(I) pref. contains nonionic and/or anionic **surface-active** agents. (I) pref. contains very finely divided insol. fillers, pigments, and water-sol, or water-insol. colourants. Fillers pref. have particle dia. 25-**100 microns** and specific surface more than 10 sq. /g, (I) contg. 2-30, partic. 2-10, kg such filler per 100 kg coating. (I) contains water-repellents, resins, setting accelerators, swelling agents, and plasticising air entrainers. (I) contains up to 10, partic. 0.05-2, kg salt of fatty acid as water-repellent.
USE/ADVANTAGE - For forming **insulation** against heat or sound. (I) adheres well and is thixotropic, coating has good appearance, shows no cracking, is waterproof, and is less dense, hence of lower wt., than coatings obtd. using cement and/or lime.

58/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004155697
WPI Acc No: 1984-301236/198449
XRAM Acc No: C84-128235
XRPX Acc No: N84-224594

Polyolefin electrical **insulation** contg. adsorbent for heavy metal ions - or ion exchange binder, reducing water treeing

Patent Assignee: SIEMENS AG (SIEI)
Inventor: HENKEL H J; MULLER N; HENKEL H; MUELLER N

Number of Countries: 018 Number of Patents: 014
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4623755	A	19861118	US 85775705	A	19850913	198649
EP 127052	B	19891004				198940

Priority Applications (No Type Date): DE 3318988 A 19830525
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3318988	A		15		
EP 127052	A	G			

Designated States (Regional): AT BE CH DE FR GB IT NL SE

Abstract (Basic): EP 127052 A

1. Polyolefine-based electrical **insulations**, more particularly in the case of cables and leads, for medium and high voltage from approximately 10 kV having an additive to retard water trees, characterized in that they contain as an additive in homogeneous distribution 0.05 to 10% by weight, as compared with the total weight, of a substance, which is active in adsorbing heavy metal ions or which binds heavy metal ions by ion exchange, having a particle size of up to 50 microns or an agglomerate size of up to **100 microns**.

(6pp)

DE 3318988 A

An electrical **insulation** based on polyolefins contains 0.05-10 wt.% of an active adsorbent for heavy metal ions or a substance which binds heavy metal ions in ion-exchange; the particle size of the additive is up to 50 microns, or the agglomerate size is up to **100 microns**.

The additive is esp. pyrogenic and/or pptd. silica, alumina and alumina hydrate with high surface activity, and/or Al silicate. The additive may be a synthetic prod.. The amt. is partic. 0.1-4 (0.5-2) wt.%. The particle size is esp. up to 20 microns. The additive may be incorporated in the polyolefin with a phlegmatising agent, pref. as a paste.

Abstract (Equivalent): US 4623755 A

Insulated electrical conductor comprises polyolefin **insulating** compsn. contg. 0.1-4 wt.% homogeneously distributed silica, alumina (hydrate) or Al silicate which is absorption active for heavy metal ions or which binds heavy metal ions in an ion exchange and which has agglomerate size up to **100 micron**.

Pref. the compsn. contains 0.5-2 wt.% pyrogenic and/or pptd. silica

or Al oxide (hydrate) with large **active surface** or Al silicate, any of which may be prepd. synthetically.

USE/ADVANTAGE - For cables and wires, having medium and high voltages e.g. 10 kV or above. Formation of water trees in the **insulating** compsn. is prevented.

58/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002520205
WPI Acc No: 1980-38234C/198021
High compressive strength shaped articles - comprising homogeneously arranged inorganic solid particles and larger densely packed particles
Patent Assignee: DENSIT AS (DENS-N); AALBORG AS (AALB-N); BACHE H H (BACH-I); AALBORG PORTLAND CEMENT FAB AS (AALB-N); DENSIT A/S (DENS-N)
Inventor: BACHE H H
Number of Countries: 021 Number of Patents: 017
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8000959	A	19800515				198021 B
EP 10777	A	19800514				198021
NO 7903532	A	19800623				198029
US 5234754	A	19930810	US 80195422	A	19800624	199333
			US 83470628	A	19830228	
			US 86880332	A	19860624	
			US 88243157	A	19880909	

Priority Applications (No Type Date): DK 792976 A 19790713; DK 784924 A 19781103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5234754	A		28	B32B-018/00	Cont of application US 80195422
					Cont of application US 83470628
					Cont of application US 86880332

Abstract (Basic): WO 8000959 A

A shaped article having a coherent matrix comprises (A) homogeneously arranged inorganic solid particles of size 50 angstroms - 0.5 mu; (B) densely packed solid particles of size 0.5-**100 mu**, which are at least one order of magnitude larger than the particles (A); and opt. (C) additional bodies having at least one dimension which is at least one order of magnitude larger than the particles (A). Particles (A) are homogeneously distributed in the void vol. between particles (B).

Bodies (C) are Portland cement.

The article can be, e.g. an in situ cast oil well wall, duct of fissure filling, sheet, panel or tile of thin-walled plane or corrugated shape, anticorrosion protecting cover applied on steel and concrete parts, pipe, tube, electrically **insulating** part, nuclear shielding or container.

Abstract (Equivalent): EP 10777 B

A process for preparing a shaped article, the process comprising combining A) inorganic solid silica dust particles of a size of from 50 angstrom to 0.5 mu.m, and B) solid particles having a size of 0.5-**100 mu**.m and being at least one order of magnitude larger than the respective particles stated under A), at least 20% by weight

Composite material for producing a shaped article consists of homogeneously arranged in organic solid particles, 50 Angstrom - 0.5 mu in size, arranged in the voids between densely packed solid particles, 0.5-**100 mu** in size, in a proportion of 0.1-50 vol.%.

12/06/2002 09/992,387

Surface active agent ensures homogeneous distribution and fluidity while liq. fills voids. Pref. inorganic particles are ultra-fine silica particles, dispersed in Portland cement particles.

12/06/2002 09/992,387

58/3,AB/8 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

05425727
MAKE-UP COSMETIC

PUB. NO.: 09-040527 [JP 9040527 A]
PUBLISHED: February 10, 1997 (19970210)
INVENTOR(s): YOSHIDA MASASHI
FUKUI HIROSHI
APPLICANT(s): SHISEIDO CO LTD [000195] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-210956 [JP 95210956]
FILED: July 27, 1995 (19950727)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a new make-up cosmetic with the improved compatibility with skin, free from offensive odor peculiar to protein by formulating a wool and or hair component into the original cosmetic.

SOLUTION: Wool and/or the hair are finely ground to <=**100.mu**.m particle size, and s-cyanoethylated to remove insoluble cuticles. The resultant hydrophilic s-cyanoethylated keratin powder is formulated into the original cosmetic preferably at 1-95wt.% to the whole weight of the make-up cosmetic. The scyanoethylated keratin is intrinsically safe for human bodies because it is keratin protein, and the make-up cosmetic which contains the s-cyanoethylated keratin has also high safety to the skin because the cosmetic contains no or scarce **surface-active** agent. In addition, this make-up cosmetic is excellent in transparency and thermal **insulation**.

58/3,AB/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03646595

ELECTROVISCOUS FLUID

PUB. NO.: 04-011695 [JP 4011695 A]
PUBLISHED: January 16, 1992 (19920116)
INVENTOR(s): MURAKAMI KAKUJI
KURAMOTO SHINICHI
NAGAI KIYOFUMI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-115388 [JP 90115388]
FILED: May 01, 1990 (19900501)
JOURNAL: Section: C, Section No. 930, Vol. 16, No. 156, Pg. 148, April 16, 1992 (19920416)

ABSTRACT

PURPOSE: To increase shearing stress obtained when an electric field is applied and decrease current density by dispersing or suspending specific particles in an electrically **insulating** liquid.

CONSTITUTION: Particles, containing a **surface active** agent but being substantially free from water, having a dissociative functional group, such as -COOM, -SO(sub 3)M, -OM, -SM, -(R(sub 1), R(sub 2), R(sub 3))NX or -(R(sub 1), R(sub 2), R(sub 3))PX(wherein M is H, an alkali metal, an ammonium or a phosphonium; R(sub 1), R(sub 2), R(sub 3) are each H or a (substituted) alkyl; and X is an element or functional group capable of forming an anion, such as halogen) in the molecule and having a particle size of 0.1-**100.mu** .m, are dispersed or suspended in an electrically **insulating** liquid, that is a liquid which has been used as an electroviscous fluid giving the Winslow effect.

58/3,AB/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

02752029

ANTISTATIC LAMINATED METAL PLATE

PUB. NO.: 01-049629 [JP 1049629 A]
PUBLISHED: February 27, 1989 (19890227)
INVENTOR(s): SAEKI KATSUHIRO
TAKIZAWA KATSUHIKO
APPLICANT(s): NIPPON STEEL METAL PROD CO LTD [000683] (A Japanese Company or Corporation), JP (Japan)
RIKEN VINYL KOGYO KK [470163] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-205234 [JP 87205234]
FILED: August 20, 1987 (19870820)
JOURNAL: Section: M, Section No. 833, Vol. 13, No. 237, Pg. 102, June 05, 1989 (19890605)

ABSTRACT

PURPOSE: To decrease the self static build-up developed by vibration and friction, and rapidly decrease and eliminate inflowing static electricity by providing an earthing point on an antistatic layer by a method wherein the antistatic layer is provided through an electrical **insulating** layer on a metal base.

CONSTITUTION: A metal base 1, which is a steel plate galvanized 2 and then chromate- treated 3, is used so as to provide an antistatic layer 5 through an adherent electrical **insulating** layer 4 onto the base 1. In order to form the electrical **insulating** layer 4 onto the metal base 1, electrical **insulating** adhesive is applied onto the base. As the electrical **insulating** adhesive, adherent resin, which has functional groups and does not contain electrically conductive material, such as acrylic resin, epoxy resin, modified vinyl resin and the like are preferable. The antistatic layer 5 is formed by adding antistatic function to the resin by blending antistatic agent with the resin. As the resin, polyolefin resin, acrylic resin, polyester resin, polyamide resin, polyvinyl chloride resin or the like is exampled. The above-mentioned resin, to which the antistatic agent such as carbon powder, copper powder, other metal powder, **surface active** agent, electrically conductive plasticizing agent or the like is added, is applied onto the electrical **insulating** layer 4. The particle diameter of the antistatic agent used is normally **100.mu**.m or less.

58/3,AB/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

02597067
THIN-FILM TRANSISTOR ARRAY

PUB. NO.: 63-213967 [JP 63213967 A]
PUBLISHED: September 06, 1988 (19880906)
INVENTOR(s): TERAO NORIYUKI
INO MASUMITSU
HIROI MASAKI
ABE SHUYA
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
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APPL. NO.: 62-048079 [JP 8748079]
FILED: March 03, 1987 (19870303)
JOURNAL: Section: E, Section No. 700, Vol. 13, No. 2, Pg. 86, January 06, 1989 (19890106)

ABSTRACT

PURPOSE: To prevent the stepped disconnection of a metallic electrode wiring and current leakage among said wiring and a source and a drain by forming an active layer region shaping a channel for a thin-film transistor by a polySi thin-film or an a-Si:H thin-film and forming the active layer region into a recessed section shaped onto a substrate surface so that the upper **surface** of the **active** layer region is conformed to the substrate surface.

CONSTITUTION: A recessed section 9 in the same area and the same depth as an active layer region are shaped to an **insulating** substrate 11 consisting of quartz, pyrex, etc. It is preferable that the recessed section 9 is formed to the rectangle of one side of 20-**100.mu**.m and depth is brought to 1000 angstroms or more. The recessed sections 9 are shaped only by the same number as the number of the active layer regions to be formed onto the **insulating** substrate 11. An active layer 5 composed of poly Si or a-Si:H is shaped into the recessed section 9 so that the upper **surface** of the **active** layer 5 is conformed to the upper surface of the **insulating** substrate 11. A gate oxide film 4, a gate electrode 6 a source 2 and a drain 3 are formed, and an inter-layer **insulating** film 7 shaped through a decompression CVD method is laminated onto these film and electrode and source and drain. A metallic electrode wiring 8 is formed onto a contact hole shaped to the inter layer **insulating** film 7.

58/3,AB/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

00830512
MANUFACTURE OF **INSULATED** COIL

PUB. NO.: 56-150812 [JP 56150812 A]
PUBLISHED: November 21, 1981 (19811121)
INVENTOR(s): CHIDAI HIDEKI
HAYASHI OSAMU
TAKADA KIYOSHI
ISOOKA TOSHIO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-053843 [JP 8053843]
FILED: April 22, 1980 (19800422)
JOURNAL: Section: E, Section No. 96, Vol. 06, No. 32, Pg. 15, February 26, 1982 (19820226)

ABSTRACT

PURPOSE: To obtain the **insulated** coil of simple manufacturing operation having superior mechanical, electrical and thermal characteristics by a method wherein after a polyamide paper being made to contain a synthetic resin dispersion liquid is wound around a coil conductor, formation is performed by heating with pressure.

CONSTITUTION: The synthetic resin like polyester resin, epoxyester resin, polyester imide resin or polyester amide imide resin, etc., is pulverized by a jet mill, etc., to form the particle having the average diameter of **100.mu**.m or less, for example, and thus obtained powder is made to disperse uniformly in water containing an anionic or a cationic **surface active** agent, and thus obtained dispersion liquid is made to be contained in a glass fiber. After the coil conductor is wound around with the polyamide paper made by mixing thus obtained wet paper type glass fiber, it is inserted in a metal mold to form by heating with pressure. Accordingly the **insulated** coil having superior electrical, mechanical and thermal characteristics can be obtained.

12/06/2002 09/992,387

61/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06113020
ELECTRONIC PART HAVING BUMP AND MOUNTING STRUCTURE THEREOF

PUB. NO.: 11-054553 [JP 11054553 A]
PUBLISHED: February 26, 1999 (19990226)
INVENTOR(s): KONDO KOJI
AOYAMA MASAYUKI
TAKEMOTO MASANORI
APPLICANT(s): DENSO CORP
APPL. NO.: 09-204729 [JP 97204729]
FILED: July 30, 1997 (19970730)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent a defective contact of an electronic part and a mounting substrate by preventing the stripping of a **solder bump** from an electrode.

SOLUTION: An outermost surface of a circuit wiring 6 formed on the surface of an **interposer** 5 **bonded** to a **solder bump** 9 is formed of ductility metal. That is to say, when the junction interface of the circuit wiring 6 and the **solder bump** 9 is formed of an alloy layer comprising metal having ductility, the alloy at the junction interface of the circuit wiring 6 and the **solder bump** 9 is not broken by stress, and the stripping of the **solder bump** 9 from the junction interface can be prevented. Thus, the defective contact between a **BGA**(**ball grid array**) package 1 and a multi-layer printed wiring substrate 3 can be prevented. In detail, in the circuit wiring 3, the part in junction with the **solder bump** 9 is constituted of **copper**, tin or palladium.

12/06/2002 09/992,387

61/3,AB/2 (Item 1 from file: 351)
DIALOG(R)File 351:Derwent WPI

012994734
WPI Acc No: 2000-166586/200015
XRPX Acc No: N00-125081
Solder bump and pad electrode connection structure in **ball grid array** - has paste made of tungsten or molybdenum filled in hole from which wiring layer is extended to connect first layer of pad electrode with electric component
Patent Assignee: NIPPONDENSO CO LTD (NPDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000022070	A	20000121	JP 98182942	A	1998062	200015	B

Priority Applications (No Type Date): JP 98182942 A 19980629
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000022070	A		8	H01L-025/00	

Abstract (Basic): JP 2000022070 A
NOVELTY - The laminated green sheets of an **interposer** (1), consists of a hole to connect the surfaces (1a,1b). A paste made of tungsten or molybdenum is filled in the hole. A wiring layer from the hole connects the layer (9a) of pad electrode to the electric components (2,4). DETAILED DESCRIPTION - A semiconductor chip (2), an electric component (3) and a thick film resistor (4) are formed on the surface (1a) of an **interposer** (1). A pad electrode (9) formed on surface (1b) is electrically connected with the electric components (2-4). The pad electrode consists of two layers (9a,9b) made of tungsten or molybdenum and **copper** plating, respectively. A **solder bump** (10) **joined** to the pad electrode electrically connects the electric component to the exterior circuit.
USE - In **ball grid array** (**BGA**) and multi-chip module (MCM).
ADVANTAGE - The durability of solder junction is increased.
DESCRIPTION OF DRAWING(S) - The figure shows explanatory diagram of multi-chip module. (1) **Interposer**; (1a,1b) **Interposer** surfaces; (2-4) Electronic components; (9) Pad electrode; (9a,9b) Layers; (10) **Solder bump**.

12/06/2002 09/992,387

65/3,AB/1 (Item 1 from file: 351)
DIALOG(R)File 351:Derwent WPI

009122170
WPI Acc No: 1992-249607/199230
XRAM Acc No: C92-111392
XRPX Acc No: N92-190694
Adhesive for reflow soldering and **encapsulation** of **flip chip** IC(s) - comprising **thermosetting** resin pref. epoxy or polyester, with fluxing agent pref. malic acid and curing agent
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: PAPAGEORGE M V; PENNISI R W
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5128746	A	19920707	US 90588888	A	19900927	199230	B
JP 4280443	A	19921006	JP 91272090	A	19910924	199246	
JP 2589239	B2	19970312	JP 91272090	A	19910924	199715	

Priority Applications (No Type Date): US 90588888 A 19900927
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5128746	A		6	H01L-023/14	
JP 4280443	A		6	H01L-021/60	
JP 2589239	B2		6	H01L-021/60	Previous Publ. patent JP 4280443

Abstract (Basic): US 5128746 A

A thermally curable adhesive is claimed, which is used for re-flow soldering of an electrical component and a substrate, the adhesive comprising (A) a thermoset resin (pref. an epoxy or polyester); (B) a fluxing agent in sufficient amt. to remove oxide coatings from the electrical component or substrate (pref. a dicarboxylic acid of formula HOOC-CH2-CRH-COOH (I); and (C) a curing agent acting on heating. R = an electron-withdrawing gp., pref. F, Cl, Br, I, S, OH, CN or benzyl.

Also claimed is an assembly comprising (1) an electrical component with a no. of electrical terminations, each including a solder bump (240); (2) a substrate (200) having terminations corresp. to the terminations of the above component; and (3) an adhesive (220) contg. components (A)-(C) as above which removes oxide coatings from the component and substrate terminations.

USE/ADVANTAGE - The adhesive is esp. useful in **encapsulating flip chip** integrated circuits; it ensures complete coverage of the die surface and allows max. use of available substrate area. The fluxing agent in the adhesive coats the solder bumps (240) and the metallisation pattern (210) and the meniscus (260) provides a continuous seal around the device periphery to protect the **active surface** from environmental contamination.